Amendments to the Specification

Please replace the paragraph beginning on page 1, line 21 with the following amended paragraph:

BIST (Built In Self Test), WRP (Weighted Random Pattern), and deterministic pattern test methodologies have evolved mainly in support of LSSD logic and structural testing, which is today the prevailing main design and test approach. Figure 1 illustrates a typical testing system [[10]] and chip design that incorporates these test methodologies. This structure utilizes a Linear Feedback Shift Register (LFSR) 12 which applies test vectors by the LFSR 12 to shift register chains 128 to 136 in an integrated circuit device under test (DUT) [[14]] 14. The outputs of the shift register chains DUT 14 are inputted into a Multiple Input Shift Register (MISR) 16.

Please replace the paragraph beginning on page 2, line 23 with the following amended paragraph:

As shown in Figure 1, in the above mentioned U.S. Pat. No 5,983,380, the self-test circuits, the pseudo random pattern generator for generating the pseudo random patterns includes weighting circuits 118 to 126 and global weight set select REG's 138 and 142 for weighting pseudo random patterns. The weighting circuits include an input 140 for receiving a weighting instruction for selectively weighting the pseudo random pattern so that the weighting circuit and the pseudo random

pattern generator generate a global weighted pseudo random pattern for testing the logic circuits.

Please replace the paragraph beginning on page 3, line 16, with the following amended paragraph:

With the above arrangement, only specific subsets of SRLs of the LSSD chain need to be weighted with each weight-set. The remaining SRLs, those not included in the weighted subset, can be loaded with "flat" pseudo-random patterns generated by the built-in LFSR. Furthermore, multiple sets of weights and associated with multiple subsets of SRLs [[and]] can also be used. From "none" to "all" the latches in the array can be modified on each scan shift cycle.

Please replace the paragraph on page 5, line 2 with the following amended paragraph:

As shown in Figure 2, a ~~multipaht~~ multipath register array 200 is placed between the LFSR and the scan chain inputs 202. The linear feedback shift register (LFSR) 125, the SRLs 128 to 136 and the signature analysis shift register (MISR) 16 remain unchanged from that of Figure 1. The register array can be an independent memory macro, an array register structure of individual latches 208, as shown here in Figure 2, or an array structure formed using a first SRL 208 of each scan chain, as shown in Figure 3. In any case, register array 200 has a storage element for each scan chain 128 to 136 that can be fully loaded directly from the LFSR 125 and individually loaded from the array port 210. As can be seen in Figures 2, 8 and 9, test support structure for the LBIST engine 212 can be located

off chip, partially on-chip, or fully on chip, respectively. Therefore it can be seen that hardware implementation of the present invention is relatively simple, requires very low circuit overhead, and can be easily incorporated into any number of existing prior art structures including the structure of Figure 1.

Please replace the Abstract on page 12 with the following amended Abstract:

~~Test apparatus provides both flat~~ Flat pseudo random test patterns are provided in combination with weighted pseudo random test patterns so that the weight applied to every latch in [[the]] a LSSD shift register (SR) chain can be changed on every cycle. This ~~apparatus fully integrates~~ enables integration of on-chip weighted pattern generation with either internal or external weight set selection. ~~With WRP test technology, the~~ WRP patterns are generated by [[the]] a tester either externally or internally to [[the]] a device under test [[DUT]] (DUT) and loaded via the shift register inputs (SRIs or WPIs) into the chip's shift register latches (SRLs). A test (or LSSD tester loop sequence) includes loading the SRLs in the SR chains with a WRP, pulsing the appropriate clocks, and unloading the responses captured in the SRLs into the multiple input signature register (MISR). Each test can then be applied multiple times for each weight set, with the weight-set assigning a weight factor or probability to each SRL. ~~The weight factor is typically of binary granularity with probabilities of:~~

~~p{"1"} = [0,... 1/8, 1/4, 1/2, 3/4,7/8, ... or 1] for similarly for p{0}.~~

~~With the above arrangement, only specific subsets of SRLs of the LSSD chain need to be weighted with each weight-set. The remaining SRLs, those not~~

~~included in the weighted subset, can be loaded with "flat" pseudo-random patterns generated by the built-in LFSR. Furthermore, multiple sets of weights and associated with multiple subsets of SRLs and also be used. From "none" to "all" the latches in the array can be modified on each scan shift cycle.~~